IN THE CLAIMS:

1. (Previously Presented) A semiconductor device comprising:

a first semiconductor chip;

a second semiconductor chip which is mounted on the first semiconductor chip;

a first electrode group which is located on the first semiconductor chip so as to be arranged along an outer periphery of the second semiconductor chip;

a second electrode group which is located on the first semiconductor chip so as to be arranged along an outer periphery of the first semiconductor chip, wherein the second electrode group surrounds the first electrode group;

a third electrode group which is located on the second semiconductor chip;

a plurality of first wires for electrically connecting the first electrode group and the third electrode group to each other;

external connection terminals which are located around the first semiconductor chip; and

a plurality of second wires for electrically connecting the second electrode group and the external connection terminals,

wherein the first semiconductor chip has a first circuit element area on which the second semiconductor chip is mounted and a second circuit element area which is positioned between the first electrode group and the second electrode group, and wherein the second semiconductor chip includes a memory circuit and the second circuit element area includes a logic circuit which are susceptible to influence of noise caused outside the logic circuit controlling the memory circuit.

2. (Previously Presented) A semiconductor device comprising:

a first semiconductor chip having a first circuit element region and a second circuit element region which is apart from the first circuit element region, and further having an intermediate region which is positioned between the first circuit element region and the second circuit element region, wherein the second circuit element region includes a logic circuit which are susceptible to influence of noise caused outside the logic circuit;

a plurality of first electrodes which are located on the first semiconductor chip;

a plurality of second electrodes which are located on the first semiconductor chip and between the second circuit element region and an outer periphery of the first semiconductor chip, so that the second circuit element region is positioned between the first electrodes and the second electrodes;

a second semiconductor chip which is mounted in the first circuit element region of the first semiconductor chip, wherein the second semiconductor chip includes a memory circuit which is controlled by the logic circuit in the second circuit element region;

a plurality of third electrodes which are located on the second semiconductor chip;

a plurality of first wires which electrically connects the first electrodes and the third electrodes to each other;

external connection terminals which are located along the outer periphery of the first semiconductor chip so that the second electrodes are positioned between the second circuit element region and the external connection terminals; and

a plurality of second wires which electrically connects the second electrodes and the external connection terminals.

3. (Original) The semiconductor device according to claim 1, wherein:

the external connection terminals are conductive leads;

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance; and

the second electrode group and the leads are electrically connected to each other by a plurality of second wires.

4. (Original) The semiconductor device according to claim 1, wherein a size of the second semiconductor chip is smaller than that of the first semiconductor chip.

5. (Original) The semiconductor device according to claim 1, wherein the first semiconductor chip and the second semiconductor chip are sealed with a resin.

6. (Original) The semiconductor device according to claim 1, wherein:

the external connection terminals are conductive leads;

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance;

the second electrode group and the leads are electrically connected to each other by a plurality of second wires;

the first semiconductor chip and the second semiconductor chip are sealed with a resin; and

the first wires and the second wires are sealed with the resin.

7. (Original) The semiconductor device according to claim 1, wherein the first semiconductor chip is formed on a support.

8.(Previously Presented) The semiconductor device according to claim 1, wherein the first electrode group and the second electrode group are located along sides of the outer periphery of the first semiconductor device.

9. (Previously Presented) The semiconductor device according to claim 1, wherein the third electrode group is located along the outer periphery of the second semiconductor chip.

10. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip having a first circuit element area, a second circuit element area surrounding the first circuit element area, a first electrode area positioned between the first circuit element area and the second circuit element area so as to surround the first circuit element area, and a second electrode area positioned at outside of the second circuit element area so as to surround the second circuit element area~~, wherein the second semiconductor chip includes a memory circuit and the second circuit element area includes a logic circuit which are susceptible to influence of noise caused outside the logic circuit controlling the memory circuit~~;

a second semiconductor chip mounted on the first circuit element area of the first semiconductor chip, wherein the second semiconductor chip includes a memory circuit and the second circuit element area includes a logic circuit which are susceptible to influence of noise caused outside the logic circuit controlling the memory circuit;

a plurality of first electrodes located on the first electrode area of the first semiconductor chip;

a plurality of second electrodes located on the second electrode area of the first semiconductor chip;

a plurality of third electrodes located on the second semiconductor chip;

a plurality of first bonding wires for electrically connecting the first electrodes and the third electrodes, respectively;

a plurality of external connection terminals electrically connected to the second electrodes, respectively; and

a plurality of second bonding wires for electrically connecting the second electrodes and the external connection terminals.

11. (Previously Presented) The semiconductor device according to claim 10, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

12. (Previously Presented) The semiconductor device according to claim 10, wherein the circuit elements susceptible to the influence of noise are analog circuit elements.

13.(Previously Presented) The semiconductor device according to claim 10, wherein the first and second semiconductor chips are sealed with a resin.

14. (Previously Presented) The semiconductor device according to claim 10, wherein the electrical connections are a plurality of wires.

15. (Previously Presented) The semiconductor device according to claim 10, wherein external connection terminals are electrically connected to the second electrodes by a plurality of wires.

16. (Previously Presented) The semiconductor device according to claim 1, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

17. (Previously Presented) The semiconductor device according to claim 1, wherein the circuit elements susceptible to the influence of noise are analog circuit elements.

18. (Previously Presented) The semiconductor device according to claim 2, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

19. (Previously Presented) The semiconductor device according to claim 2, wherein the circuit elements susceptible to the influence of noise are analog circuit elements.

20. (Previously Presented) The semiconductor device according to claim 2, wherein the first and second semiconductor chips are sealed with a resin.

21. (Previously Presented) The semiconductor device according to claim 5, wherein a distance between an upper surface of the second semiconductor chip and an upper surface of the resin is greater than a thickness of the second semiconductor chip.

22. (Previously Presented) The semiconductor device according to claim 13, wherein a distance between an upper surface of the second semiconductor chip and an upper surface of the resin is greater than a thickness of the second semiconductor chip.